

Breaking the bottleneck: the future of AI computing with optical interconnects



Early days  
(1992 - 2014)



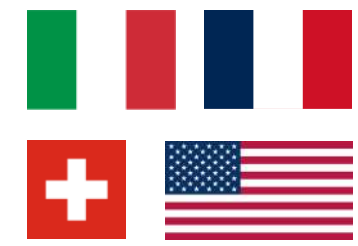
## About me



Master  
(2014 - 2016)



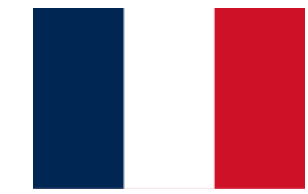
Politecnico di Torino



PhD  
(2017 - 2021)



Université de Paris

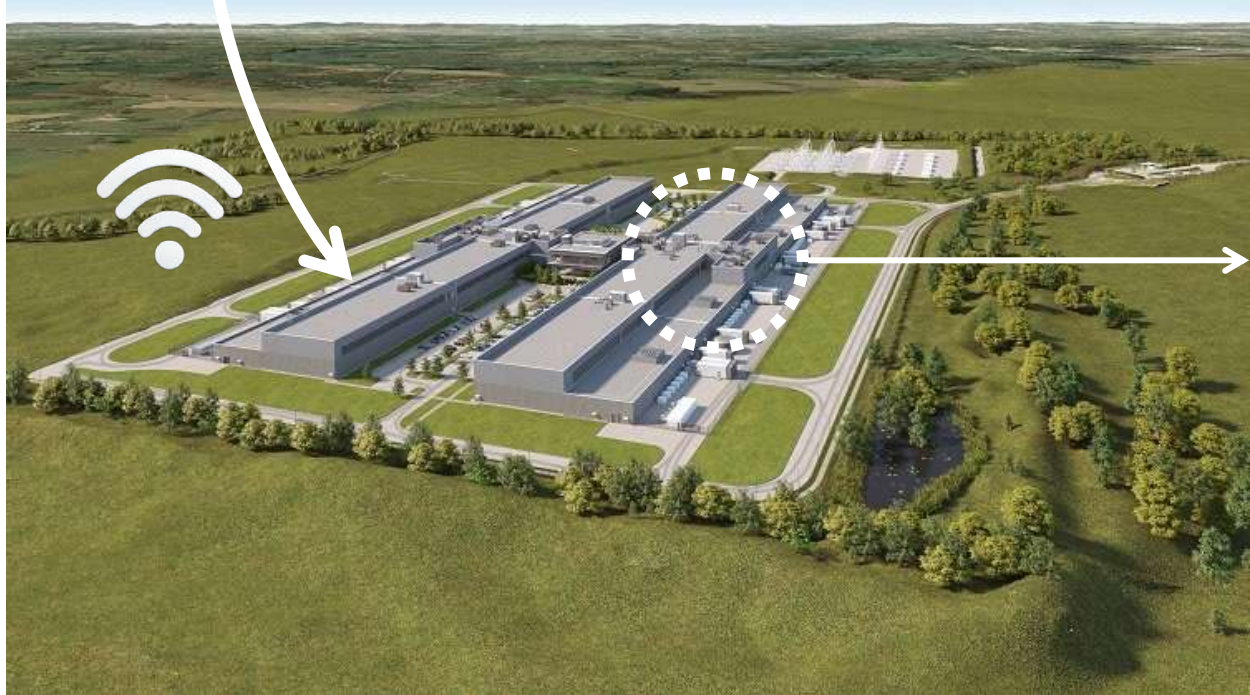


Pro life  
(2021 -)

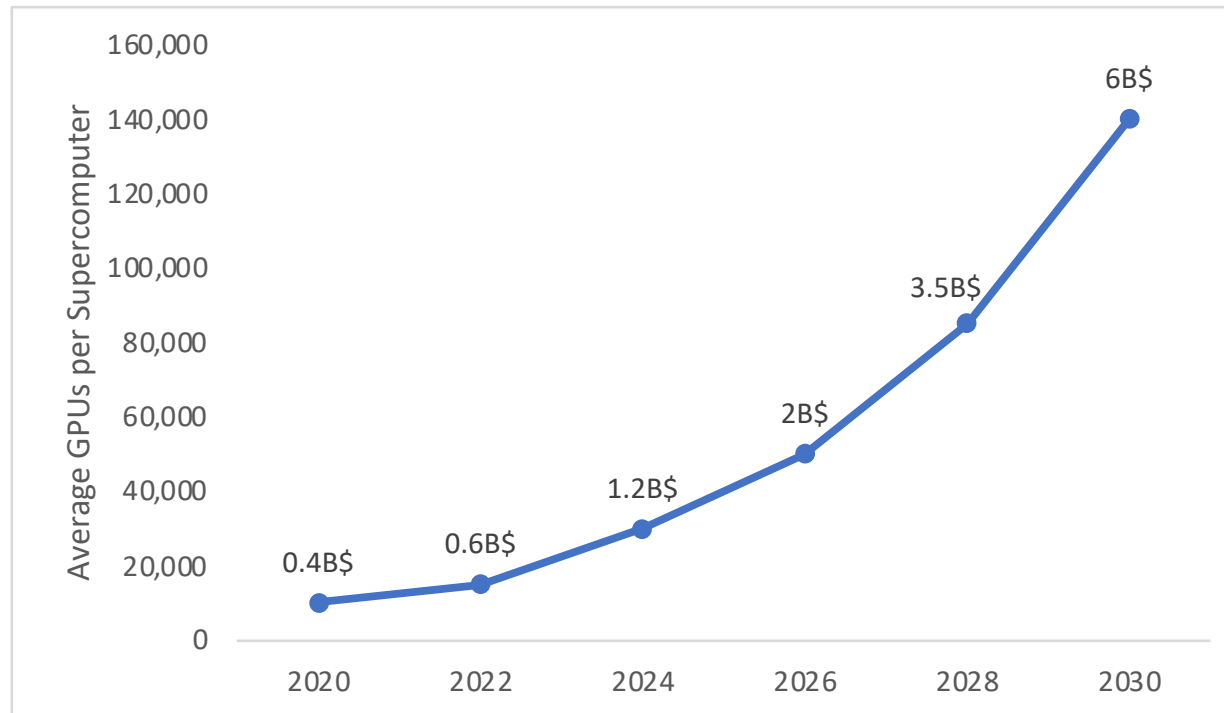




# What's behind ChatGPT?

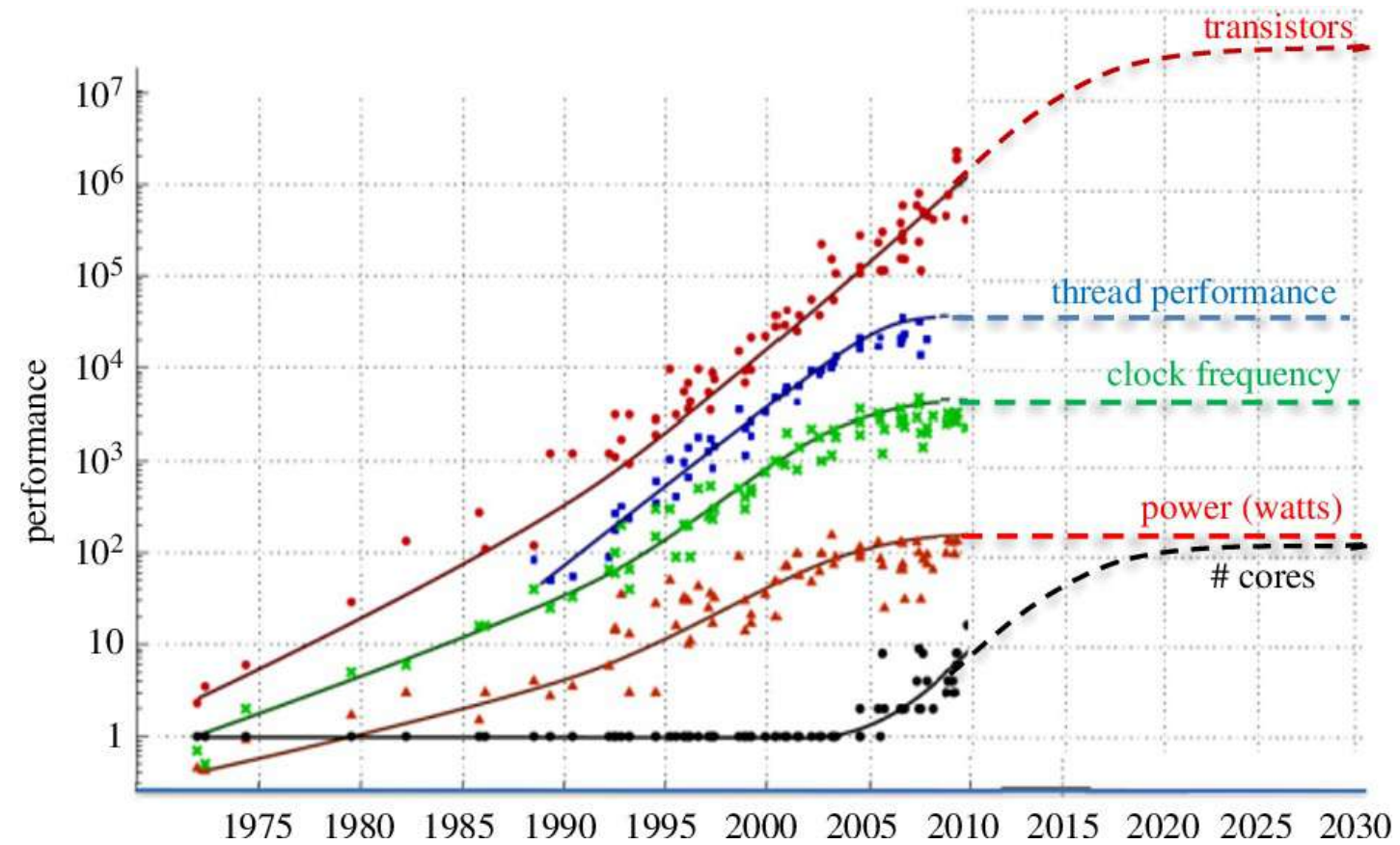


# GenAI triggered extraordinary investments in supercomputing clusters

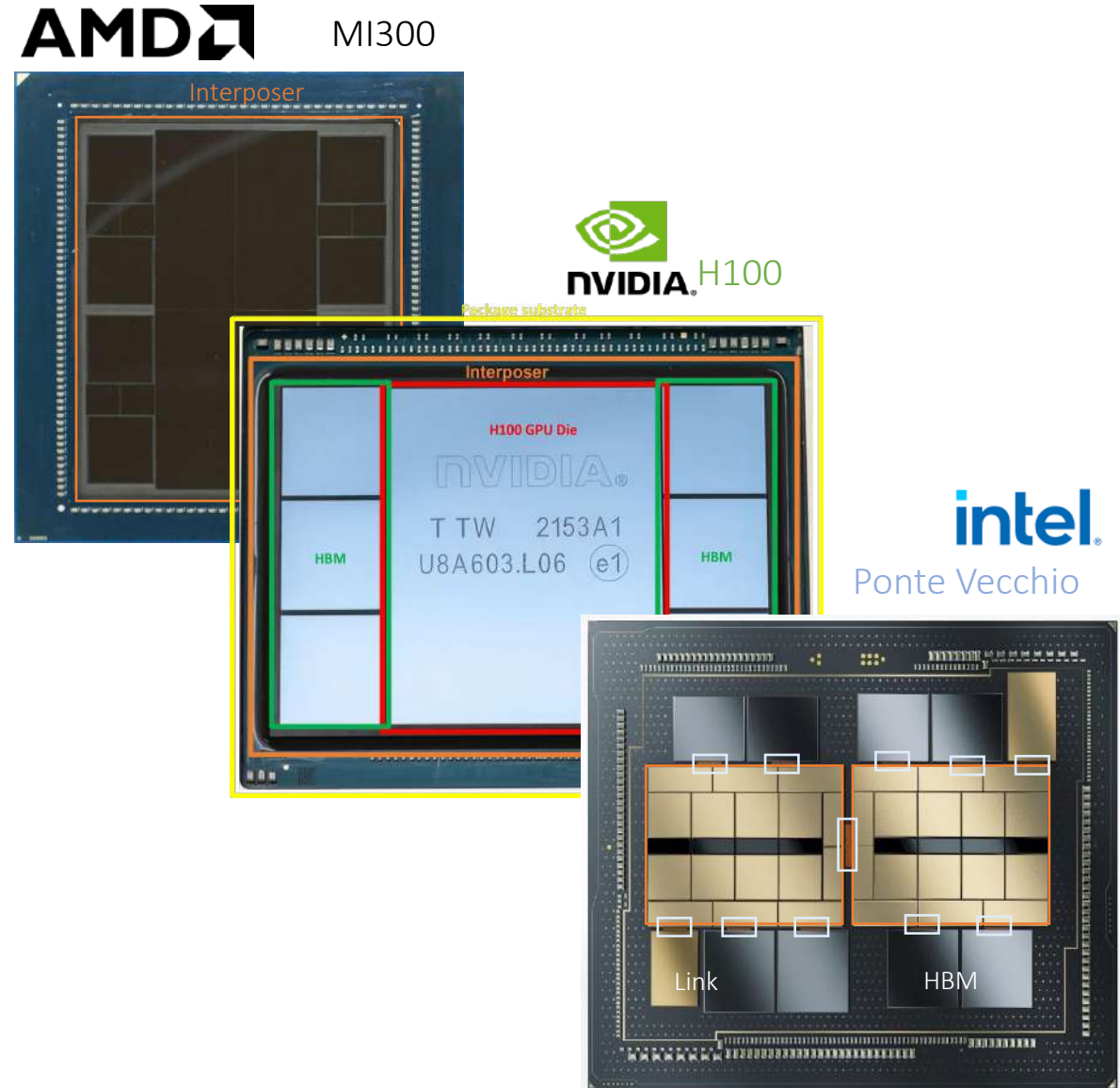
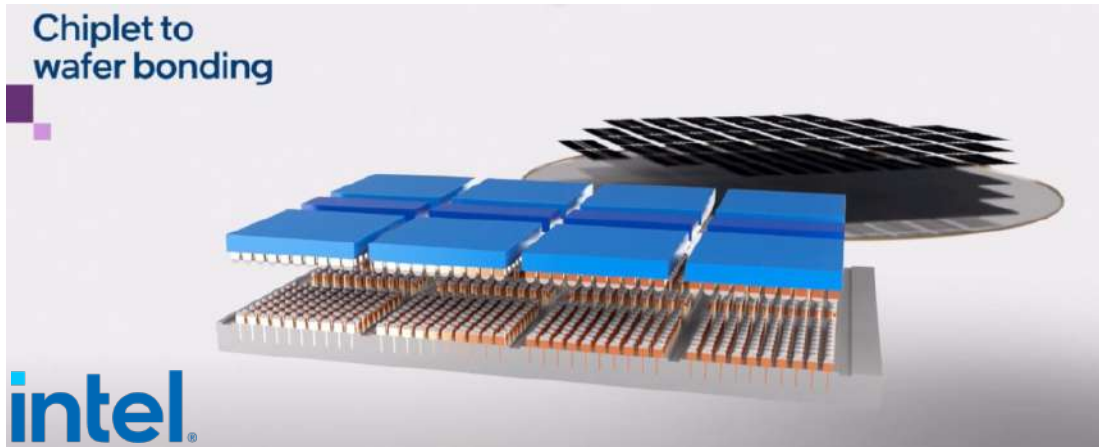




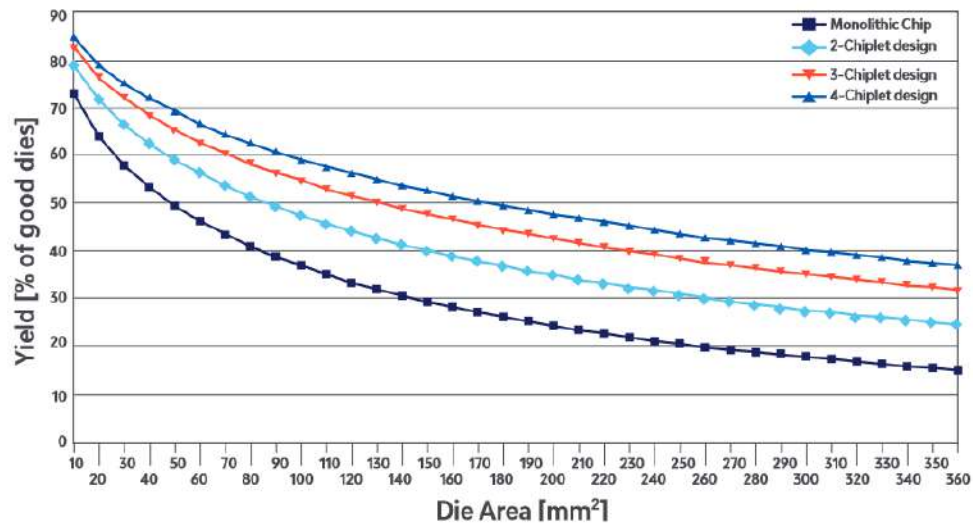
# Moore's Law is over



# The industry is pivoting to disaggregated chiplet-based solutions

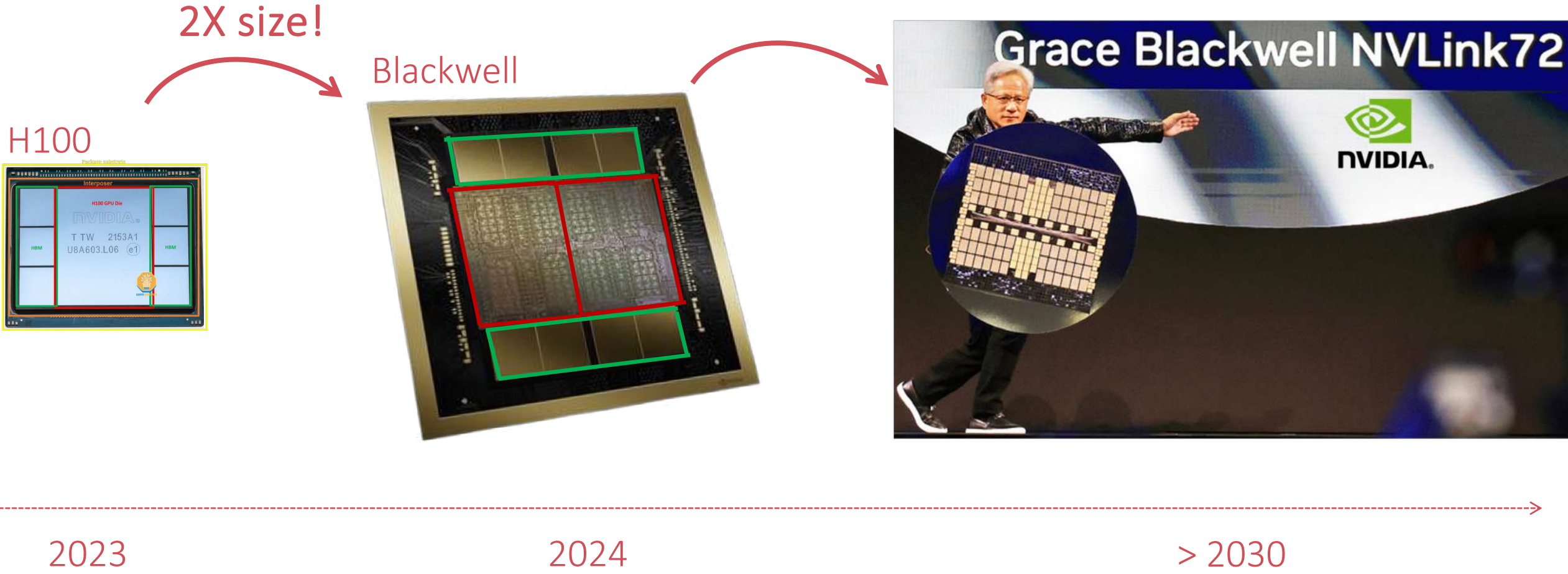


Increasing chip size comes at a cost (yield, design)

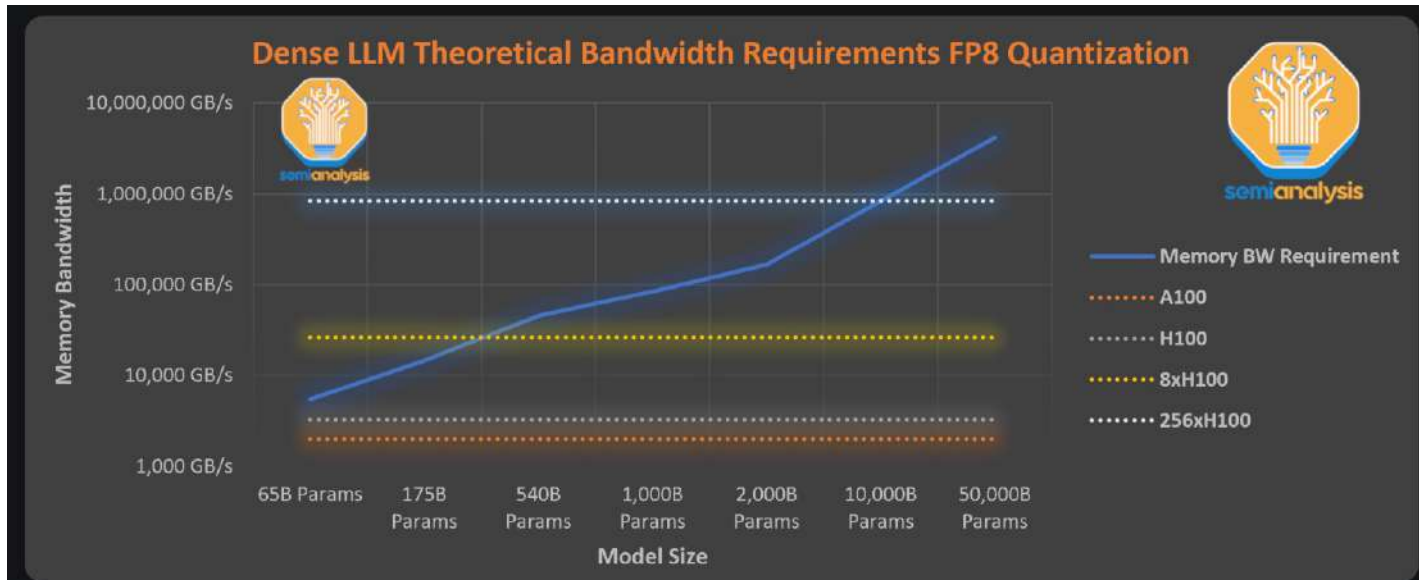




# New processors need more dies (silicon) for their circuits ...



... and GPUs need to be kept busy all the time!



This chart assumes inefficiencies from not being able to fuse every op, memory bandwidth required for the attention mechanism, and hardware overhead are equivalent to parameter reads. In reality, even with “optimized” libraries such as [Nvidia's FasterTransformer library](#), the total overhead is even larger.

The chart above demonstrates the memory bandwidth required to inference an LLM at high enough throughput to serve an individual user. It shows that even 8x H100 cannot serve a 1 trillion parameter dense model at 33.33 tokens per second. Furthermore, the **FLOPS utilization rate** of the 8xH100's at 20 tokens per second **would still be under 5%**, resulting in horribly high inference costs. Effectively there is an inference constraint around ~300 billion feed-forward parameters for an 8-way tensor parallel H100 system today.

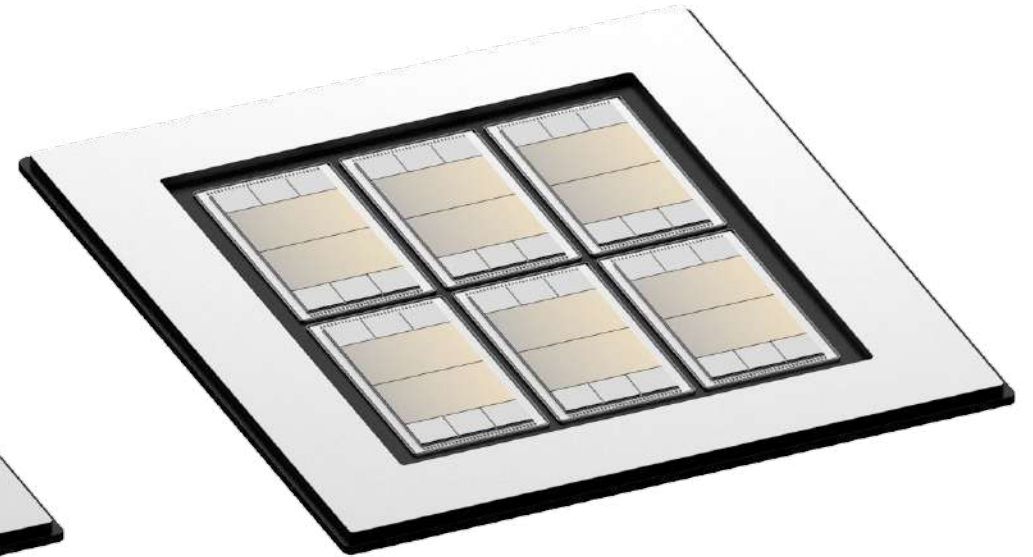
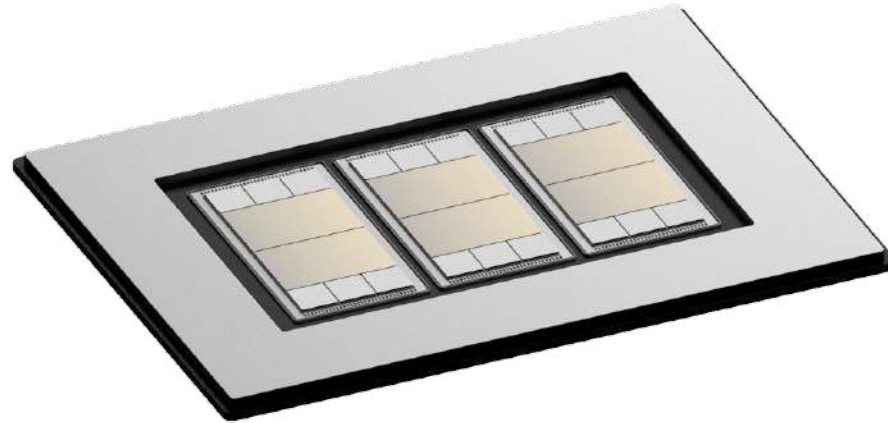
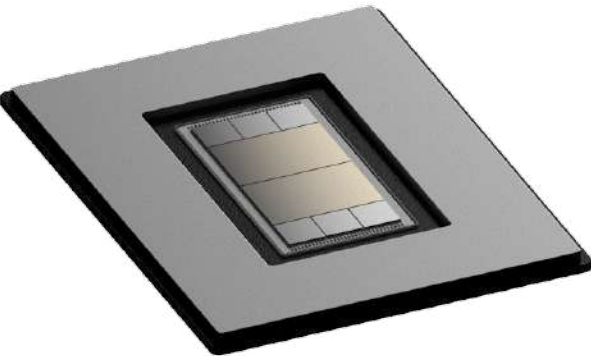


# Copper limits reach, bandwidth and energy efficiency!

|                                    |     |
|------------------------------------|-----|
| BW Density (Tbps/mm <sup>2</sup> ) | 2   |
| Reach (mm)                         | 2   |
| Energy efficiency (pJ/bit)         | 0.5 |

|                                    |     |
|------------------------------------|-----|
| BW Density (Tbps/mm <sup>2</sup> ) | 2   |
| Reach (mm)                         | 20  |
| Energy efficiency (pJ/bit)         | 3.5 |

|                                    |     |
|------------------------------------|-----|
| BW Density (Tbps/mm <sup>2</sup> ) | 2   |
| Reach (mm)                         | 200 |
| Energy efficiency (pJ/bit)         | 15  |



2024

2028

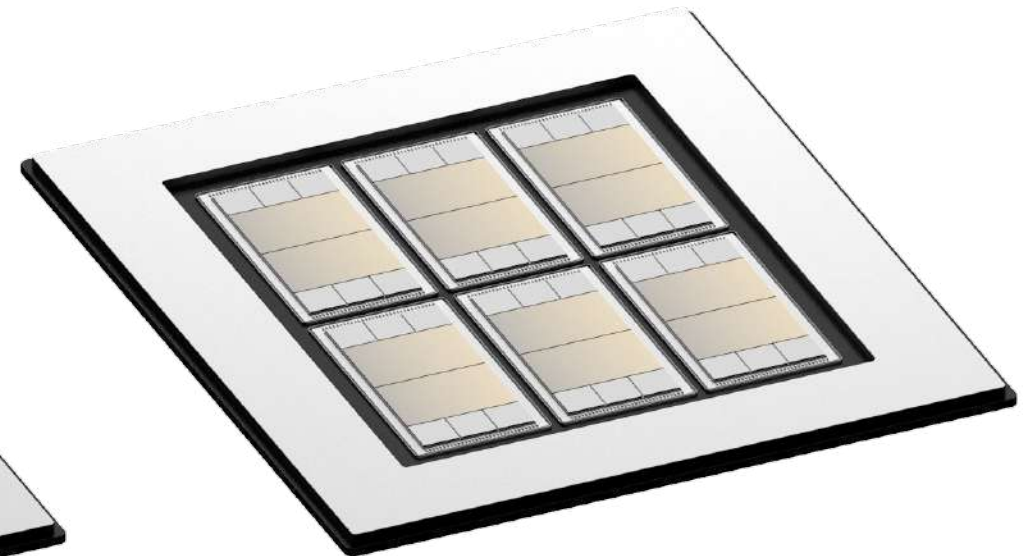
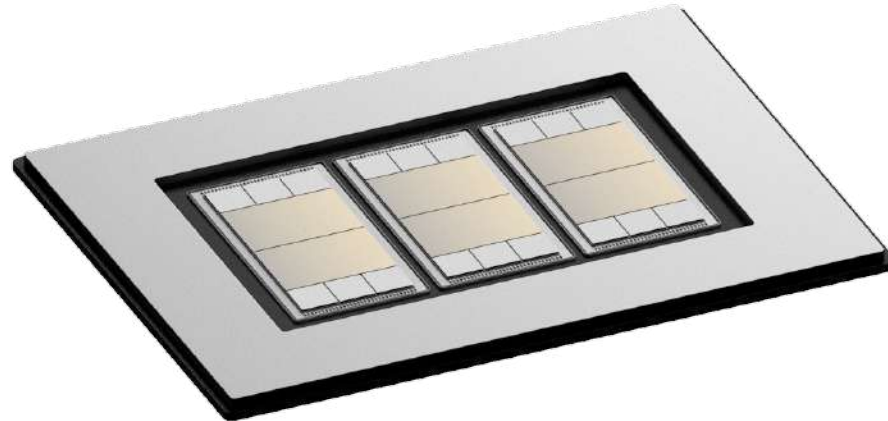
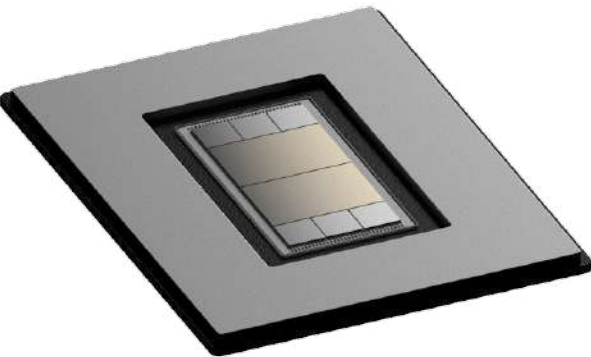
> 2030

# Copper limits reach, bandwidth and energy efficiency!

|                                    |     |
|------------------------------------|-----|
| Energy efficiency (pJ/bit)         | 0.5 |
| Reach (mm)                         | 2   |
| BW Density (Tbps/mm <sup>2</sup> ) | 2   |

|                                    |     |
|------------------------------------|-----|
| Energy efficiency (pJ/bit)         | 0.5 |
| Reach (mm)                         | 20  |
| BW Density (Tbps/mm <sup>2</sup> ) | 0.3 |

|                                    |      |
|------------------------------------|------|
| Energy efficiency (pJ/bit)         | 0.5  |
| Reach (mm)                         | 200  |
| BW Density (Tbps/mm <sup>2</sup> ) | 0.07 |



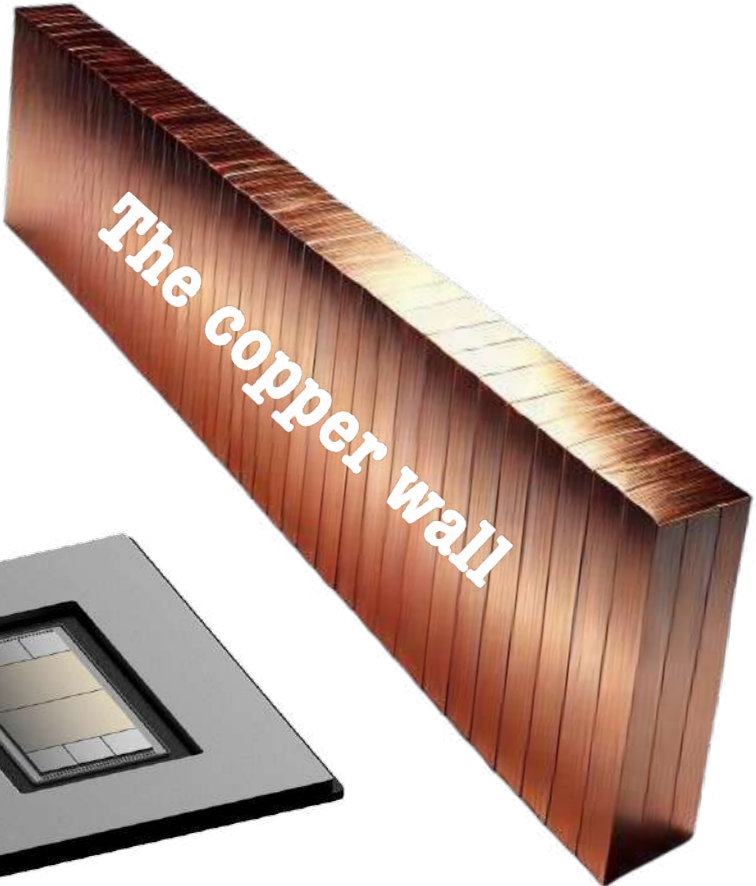
2024

2028

> 2030



# Copper limits reach, bandwidth and energy efficiency!



2024

2028

> 2030

# Photonics is THE way

Transoceanic communication (80s)  
> 10<sup>3</sup> km range



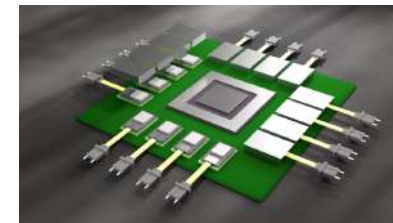
Local Area Network (early 2000s)  
~km range



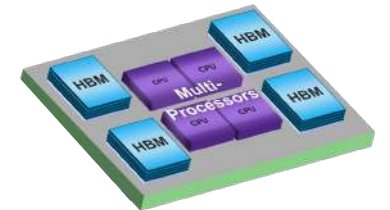
Intra-datacenter pluggable transceivers (2010s)  
~m range



Co-packaged optics (now)  
~m range



SiP die-to-die connectivity (~2030)  
≤1 cm range

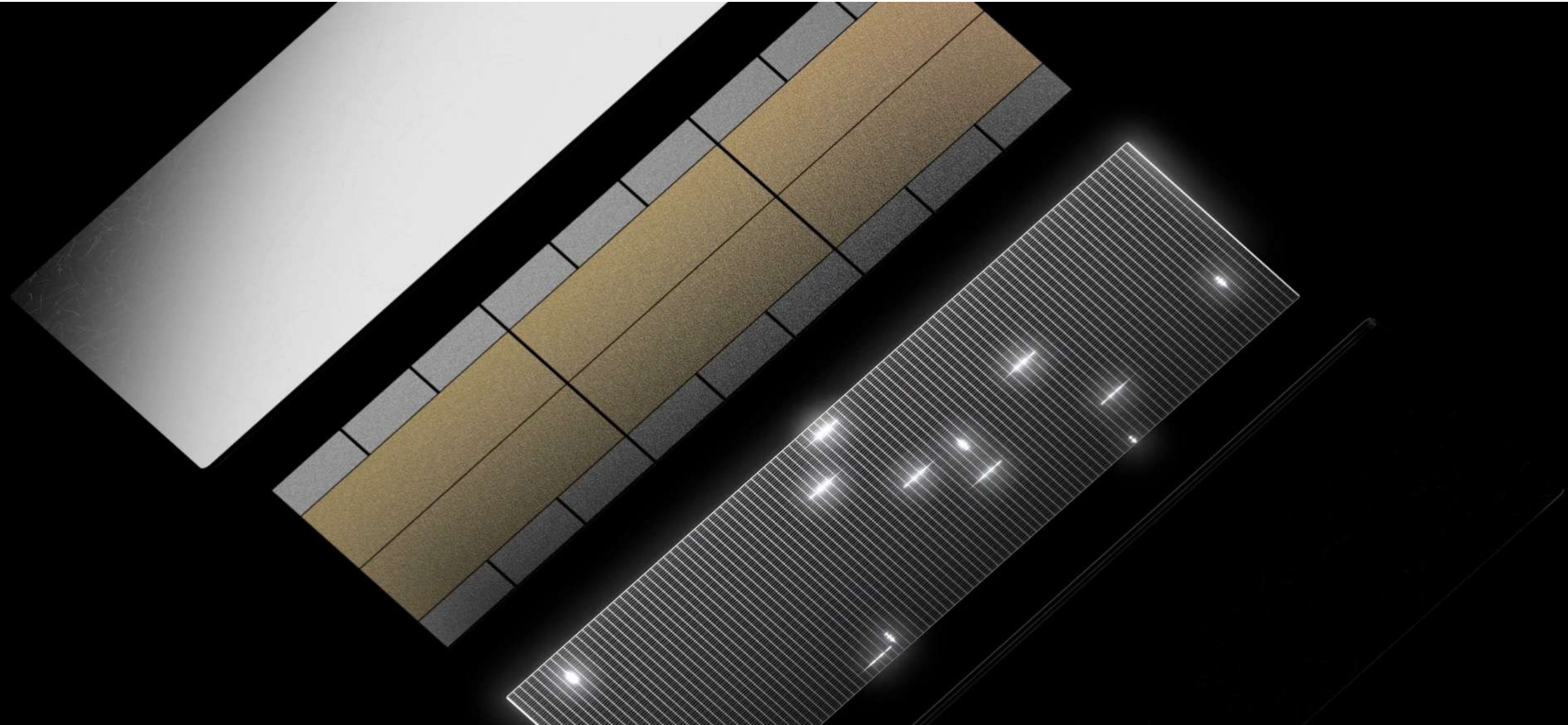


*Bandwidth demand*

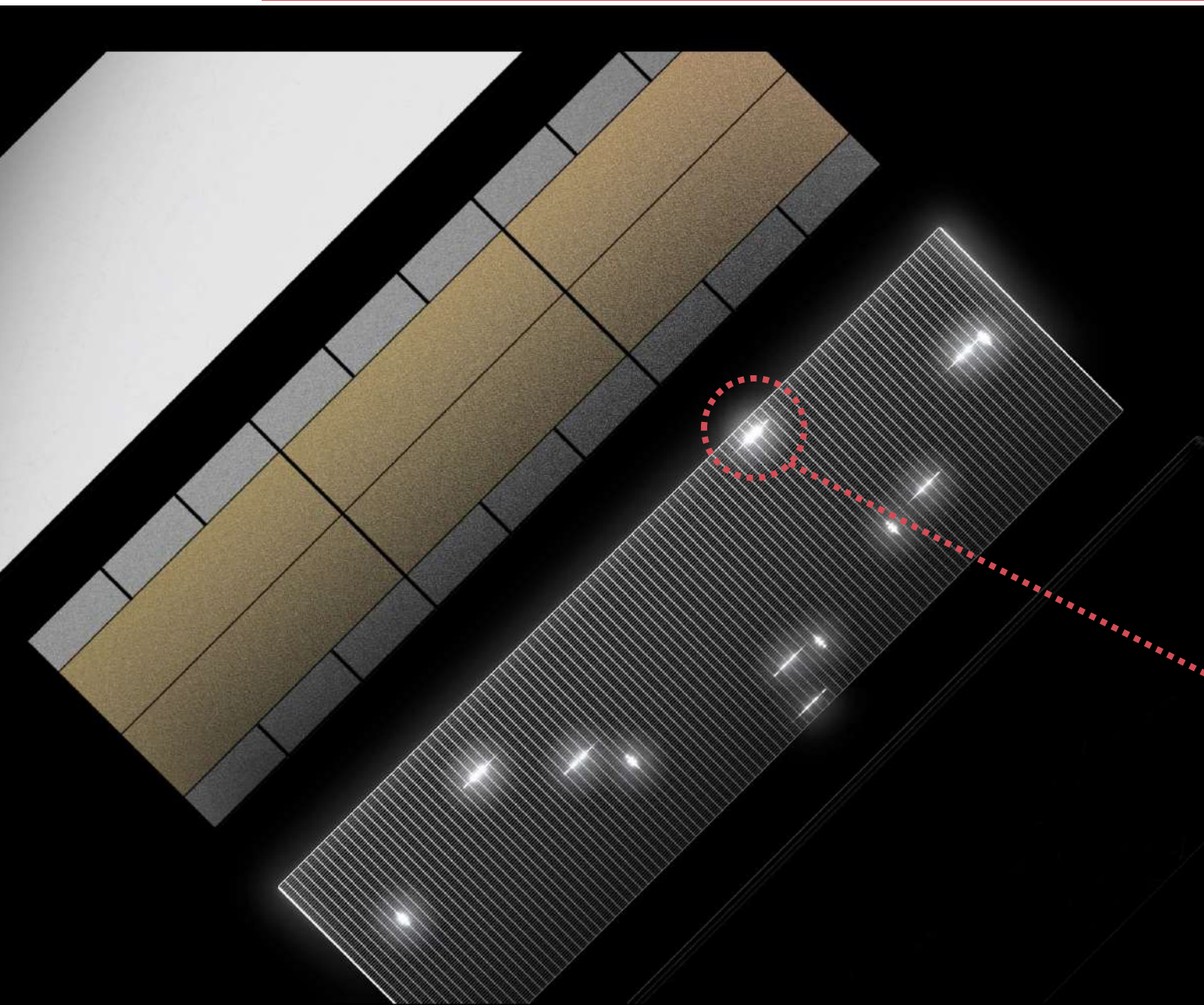


# Introducing NConnect: the optical network powered by the world's smallest laser

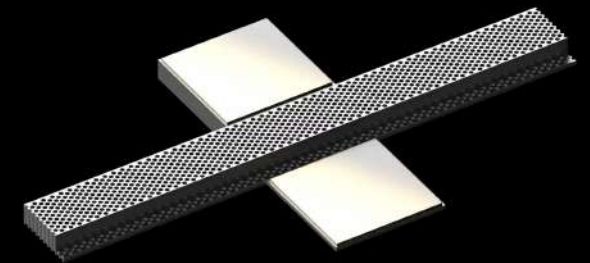
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# Our unique technology results from >15 years of research @ C2N-CNRS

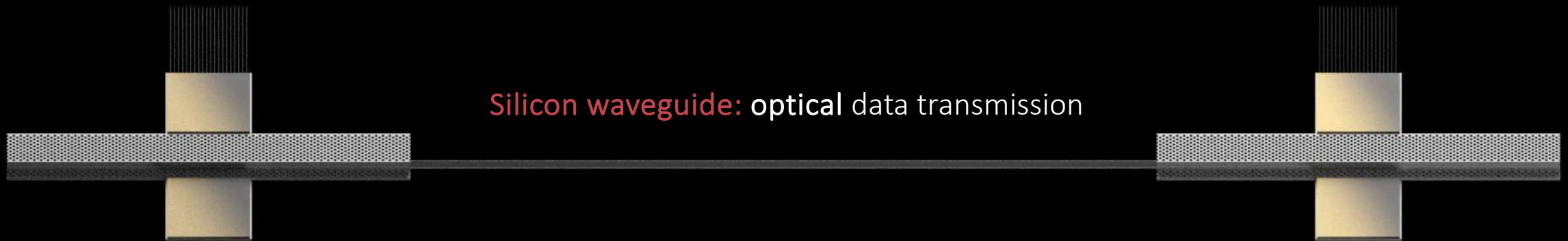
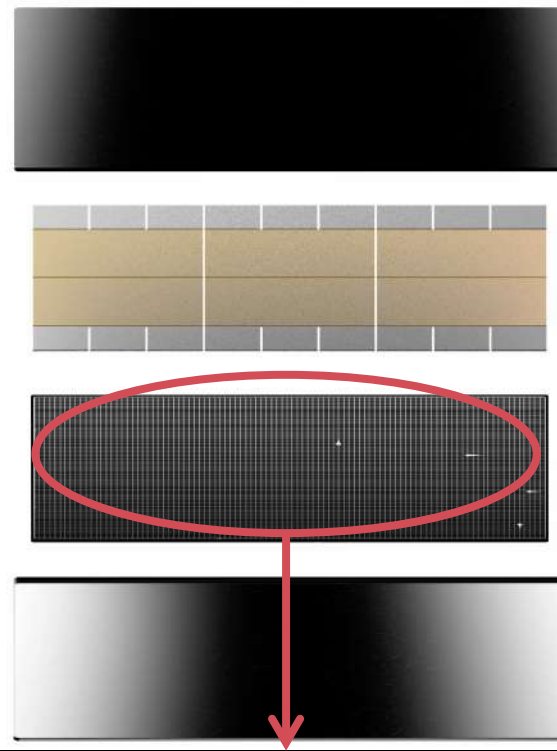


- › The **world's smallest laser** integrated on silicon (x500 smaller than industrial state-of-the-art lasers)
- › **CMOS-compatible** process → Viable production and unique reliability





# How does it work?



**Silicon waveguide:** optical data transmission

**Nanolaser:** electro-optical signal conversion

**Nanodetector:** opto-electronic signal conversion

# Our technology works with existing chiplet architectures



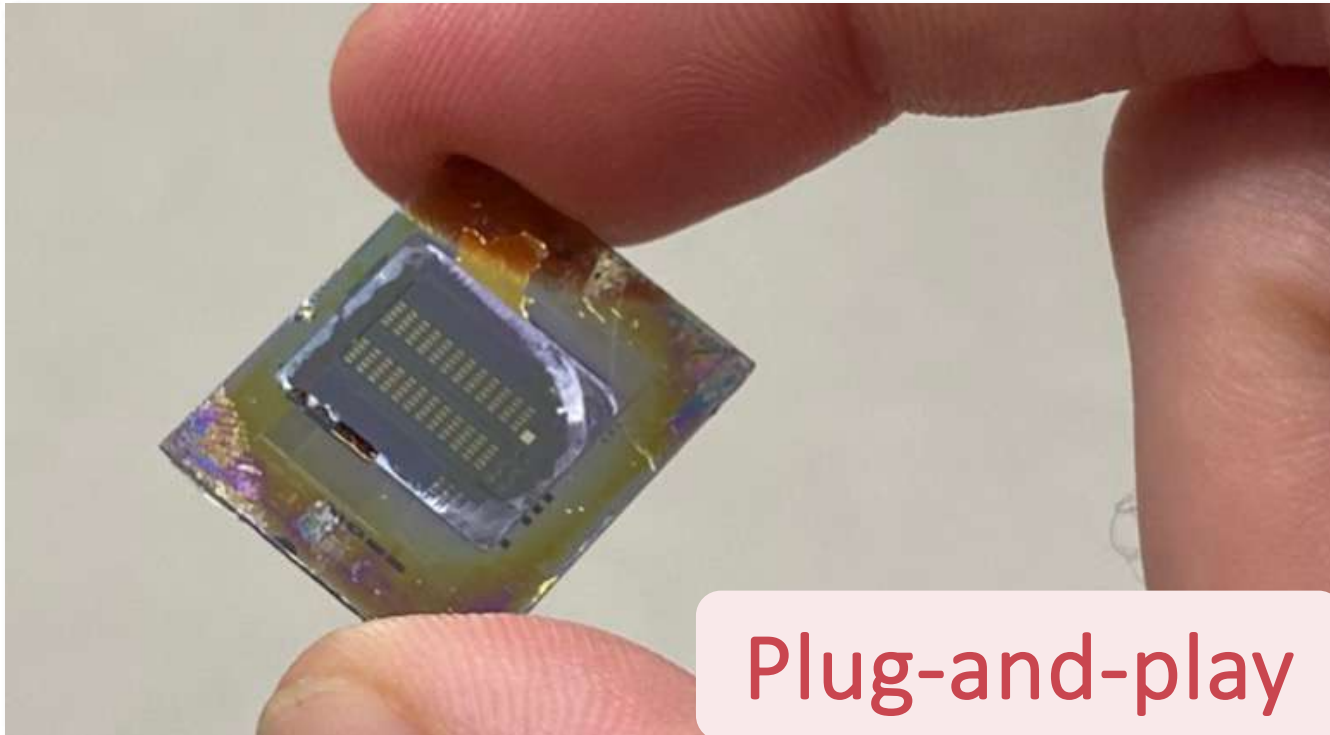
**OPEN**  
Compute Project

**Bunch of Wires (BoW) PHY Specification**

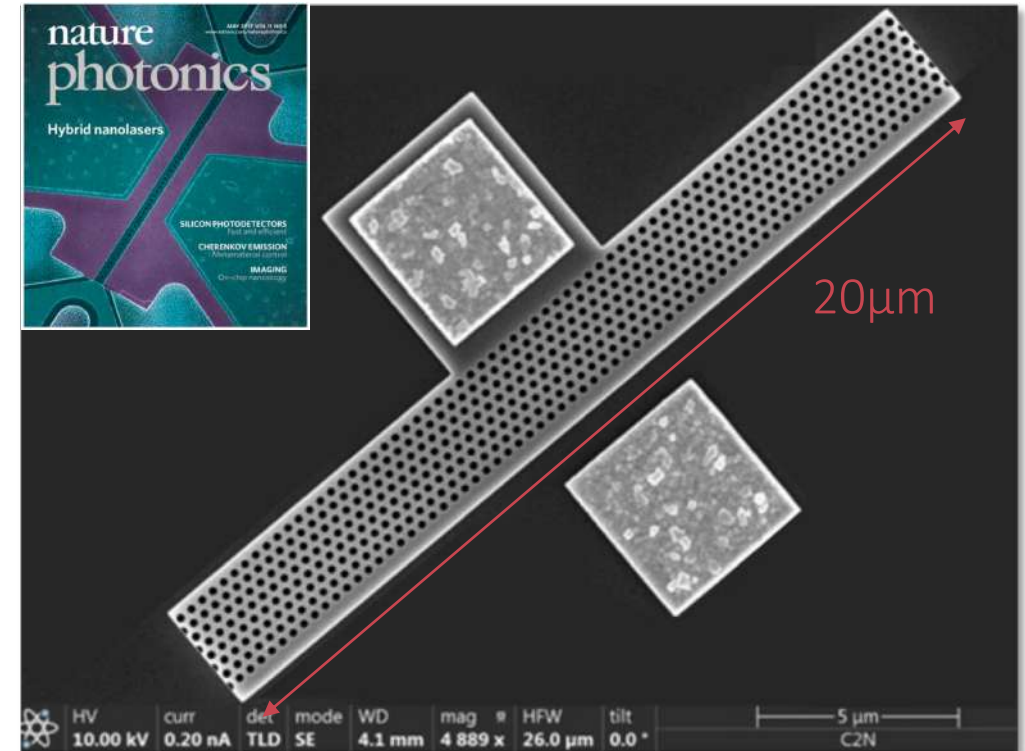
The Open Domain-Specific Architecture BoW Workstream



**Advanced Interface Bus (AIB)  
Specification**

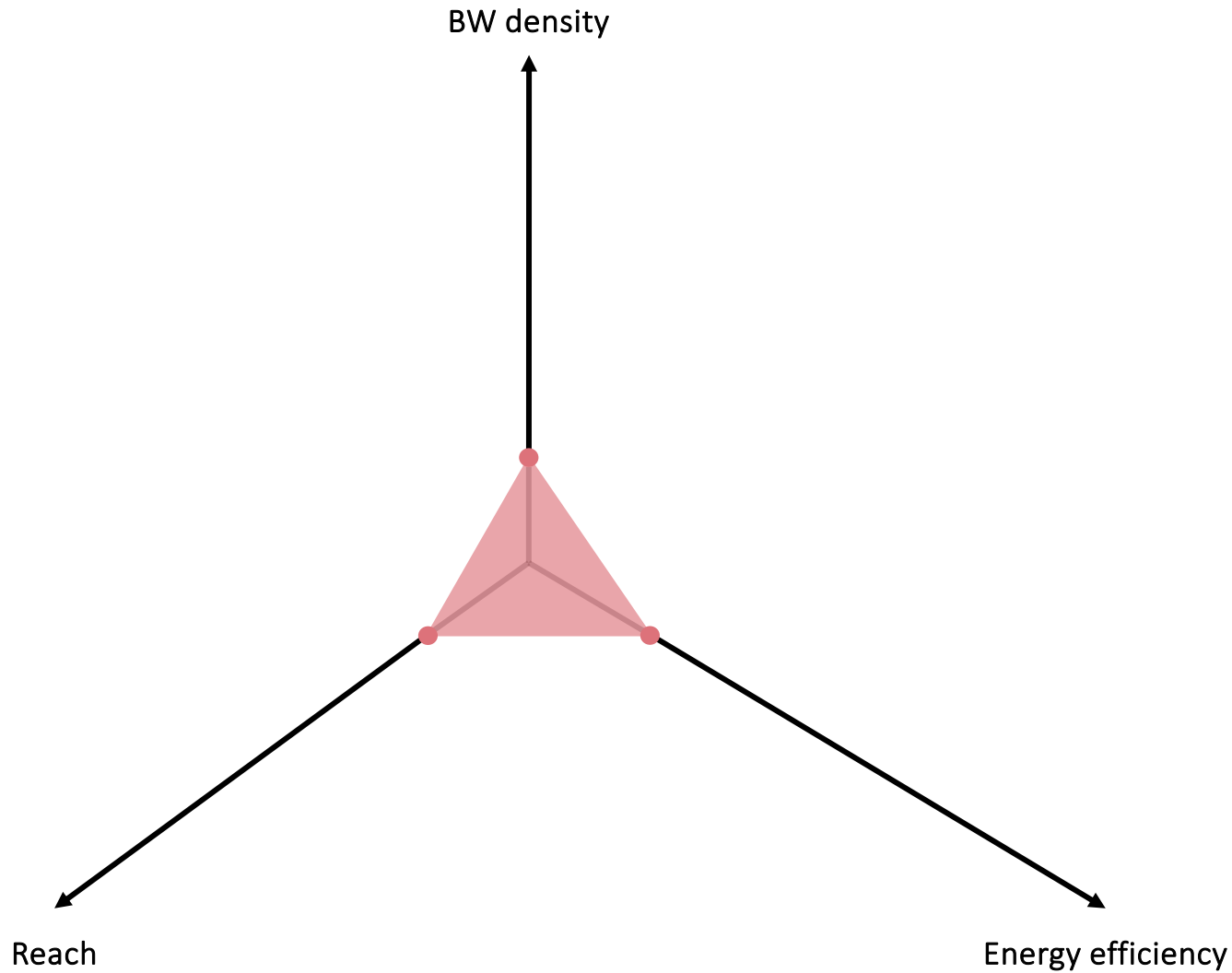


**Plug-and-play**



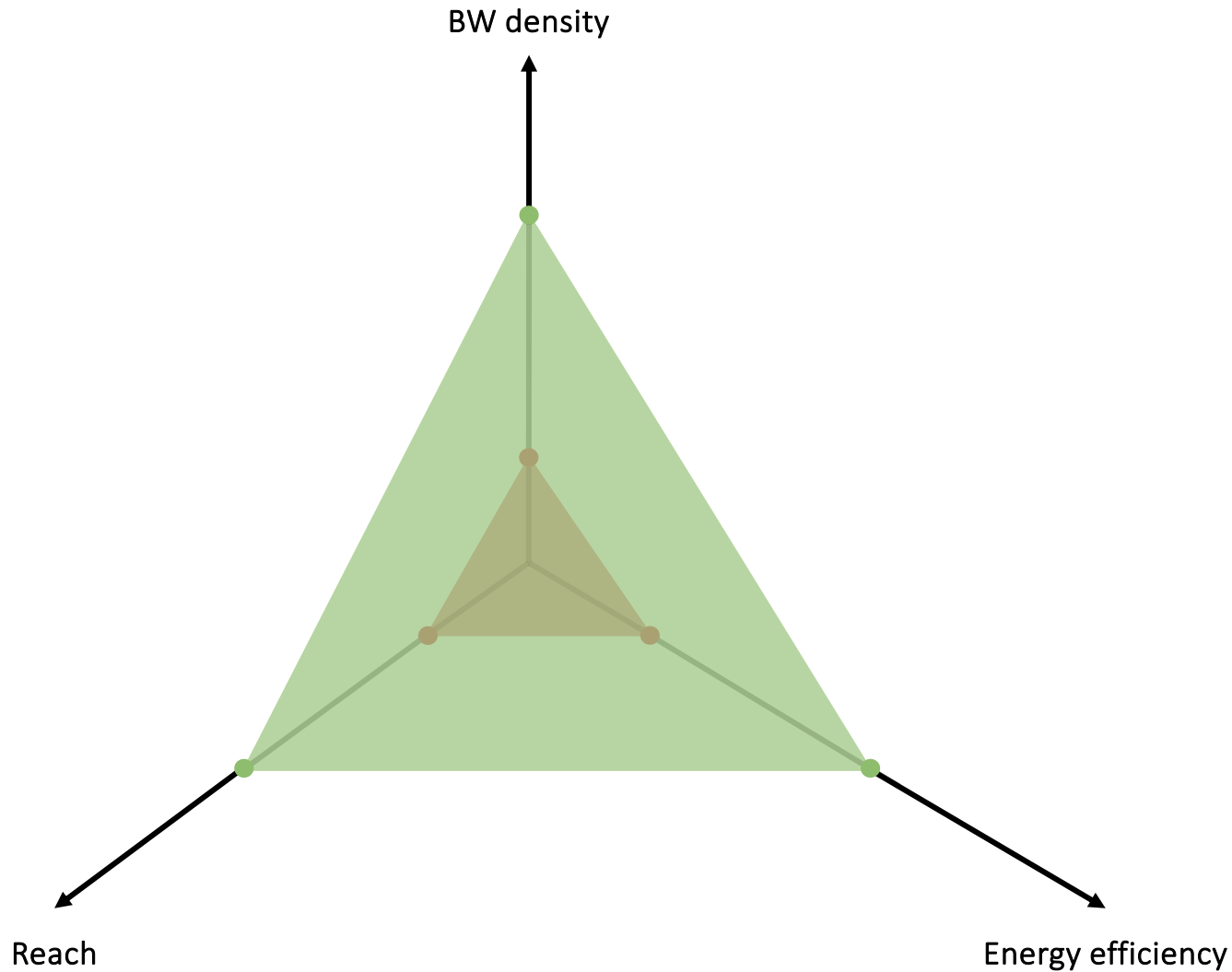


# NcodiN solves the interconnect bottleneck limitations all at once ...



| Figure of Merit                    | Copper                         |
|------------------------------------|--------------------------------|
| BW Density (Tbps/mm <sup>2</sup> ) | 2                              |
| Reach (mm)                         | 2                              |
| Energy efficiency (pJ/bit)         | 0.5                            |
| Communication system               | Point-to-Point (bidirectional) |

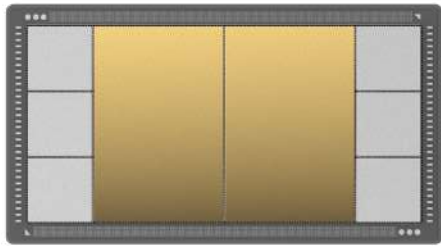
# ... through an Optical Network-On-Chip with superior performance



| Figure of Merit                    | Copper                         | <b>Ncodiv</b>                      |
|------------------------------------|--------------------------------|------------------------------------|
| BW Density (Tbps/mm <sup>2</sup> ) | 2                              | ≥60                                |
| Reach (mm)                         | 2                              | ≥50                                |
| Energy efficiency (pJ/bit)         | 0.5                            | <0.1                               |
| Communication system               | Point-to-Point (bidirectional) | <b>Point-to-All (broadcasting)</b> |

# We enable new horizons in the design space

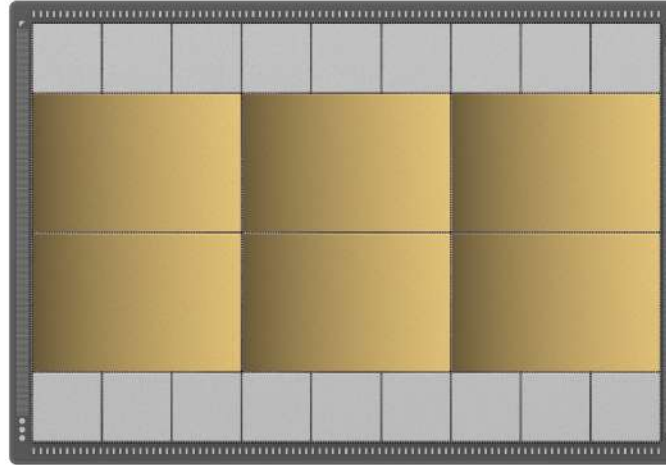
*Elec I/O-based standard package*



+

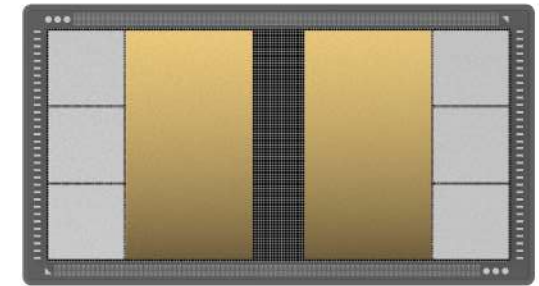
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1) "Super-package"



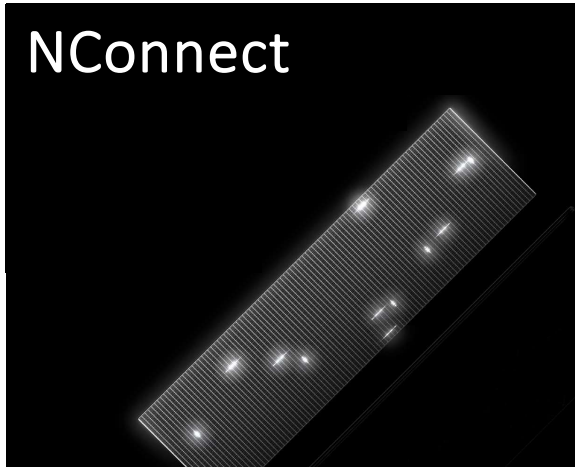
\$/performance ↑

2) Larger distance

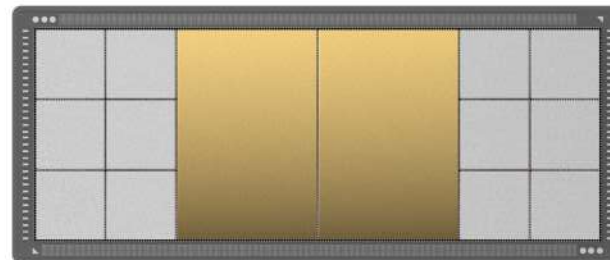


Warpage ↓

NConnect



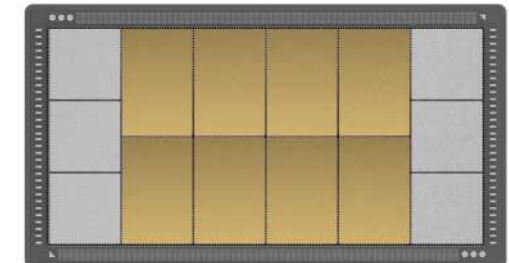
3) More memory



Memory capacity ↑

HBM warpage ↓

4) Enhanced disaggregation



Yield ↑

Design flexibility ↑



# The only photonic solution allowing to scale on-interposer copper

| <i>In-package interconnects<br/>(2.5D die-to-die)</i> |  + Copper |  |  |  |   |
|---|--|---|---|---|---|
| Manufacturing viability                               | ✓  | ✓   | ✗   | ✗   | ✗ |
| Plug-and-play capability                              | ✓  | ✓   | ✗   | ✗   | ✗ |
| Scalability   | ✓  | ✗   | ✗   | ✗   | ✗ |

“

*You have the most suited solution to break the power/reach tradeoff for on-interposer copper links.*

*Other photonics players cannot be competitive on your use-case: if a solution helps increase the bandwidth inefficiently in terms of cost and power, it will never be adopted.*

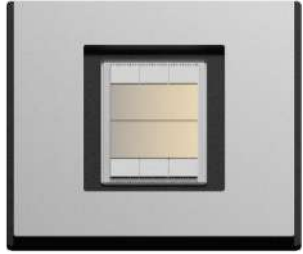
”

Director Photonics Products



# The only photonic solution allowing to scale on-interposer copper

## From today's packaging ...



|                         | Copper |
|-------------------------|--------|
| Bandwidth demand (Tbps) | 80     |
| Power (W)               | 25     |
| Cost (\$)               | 500    |

### In-package interconnects (2.5D die-to-die)

|                          | Nvidia + Copper | LIGHTMATTER | celestial AI | AVICENA |
|--------------------------|-----------------|-------------|--------------|---------|
| Manufacturing viability  | ✓               | ✗           | ✗            | ✗       |
| Plug-and-play capability | ✓               | ✗           | ✗            | ✗       |
| Scalability              | ✓               | ✗           | ✗            | ✗       |



*You have the most suited solution to break the power/reach tradeoff for on-interposer copper links.*

*Other photonics players cannot be competitive on your use-case: if a solution helps increase the bandwidth inefficiently in terms of cost and power, it will never be adopted.*



Director Photonics Products



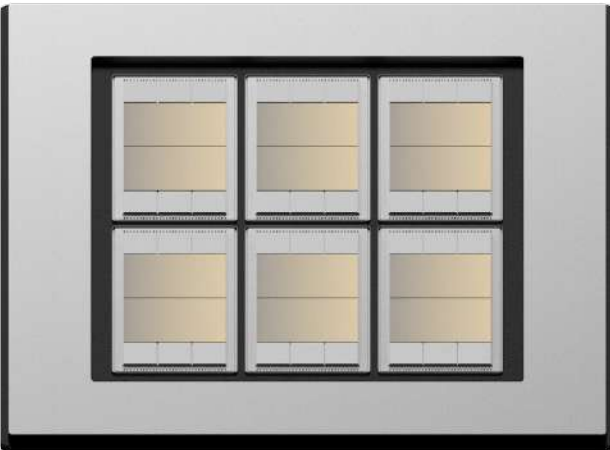
# The only photonic solution allowing to scale on-interposer copper

## From today's packaging ...



|                         | Copper |
|-------------------------|--------|
| Bandwidth demand (Tbps) | 80     |
| Power (W)               | 25     |
| Cost (\$)               | 500    |

## ... to scaled architecture



|                         | NcodiN + Copper | LIGHTMATTER | celestial AI | AVICENA |
|-------------------------|-----------------|-------------|--------------|---------|
| Bandwidth demand (Tbps) | 300             |             |              |         |
| Power (W)               | 15 + 50         | 1500        | 900          | 300     |
| Cost (\$)               | 1000 + 1000     | 150 000     | 90 000       | 30 000  |

*In-package interconnects (2.5D die-to-die)*

|                          | NcodiN + Copper | LIGHTMATTER | celestial AI | AVICENA |
|--------------------------|-----------------|-------------|--------------|---------|
| Manufacturing viability  | ✓               | ✗           | ✗            | ✗       |
| Plug-and-play capability | ✓               | ✗           | ✗            | ✗       |
| Scalability              | ✓               | ✗           | ✗            | ✗       |



*You have the most suited solution to break the power/reach tradeoff for on-interposer copper links.*

*Other photonics players cannot be competitive on your use-case: if a solution helps increase the bandwidth inefficiently in terms of cost and power, it will never be adopted.*



Director Photonics Products



✓ X100 Energy efficient  
 ✓ X100 Cost efficient



# A complementary team of nanophotonics pioneers ...



**Francesco Manegatti**

CEO and co-founder

PhD in physics, optoelectronic nanodevices  
5+ years experience in nanophotonics



**Bruno Garbin**

CTO and co-founder

PhD in physics, Neuromorphic Optical Systems (NOS)  
10+ years on experimental optics and NOS



**Fabrice Raineri**

CSO and co-founder

Full Professor, 20+ years in nanophotonics  
Pioneering research on optoelectronic nanodevices



**Carlo Guareschi**

Head of BizDev

30+ years experience in semiconductor industry



**Yacine Halioua**

Head of ProdDev

10+ years experience in semiconductor industry



## Team highlights

Team size 🙌

18

R&D, BizDev,  
Prod. Dev., HR

Upcoming →  
SOON

2

R&D, Prod. Dev.

# ... working with expert advisors and partners



**Léo Apotheker**

International executive  
previous CEO at



& board member at



**Eric Meurice**

International executive  
previous CEO at



& board member at



**Jean-Pascal Tricoire**

International executive  
previous CEO at



& board member at



**Ashkan Seyed**

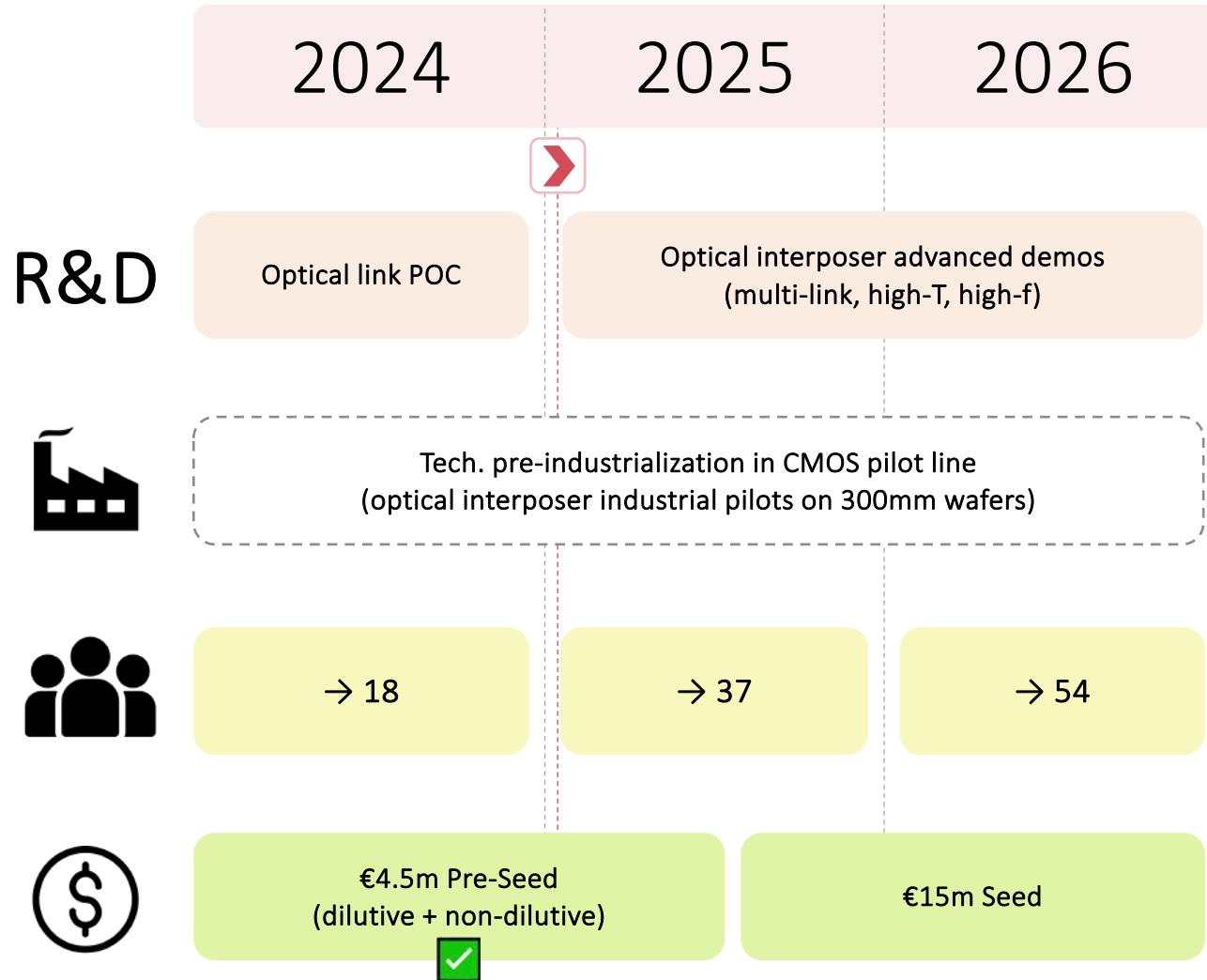
Director of Silicon Photonics  
product



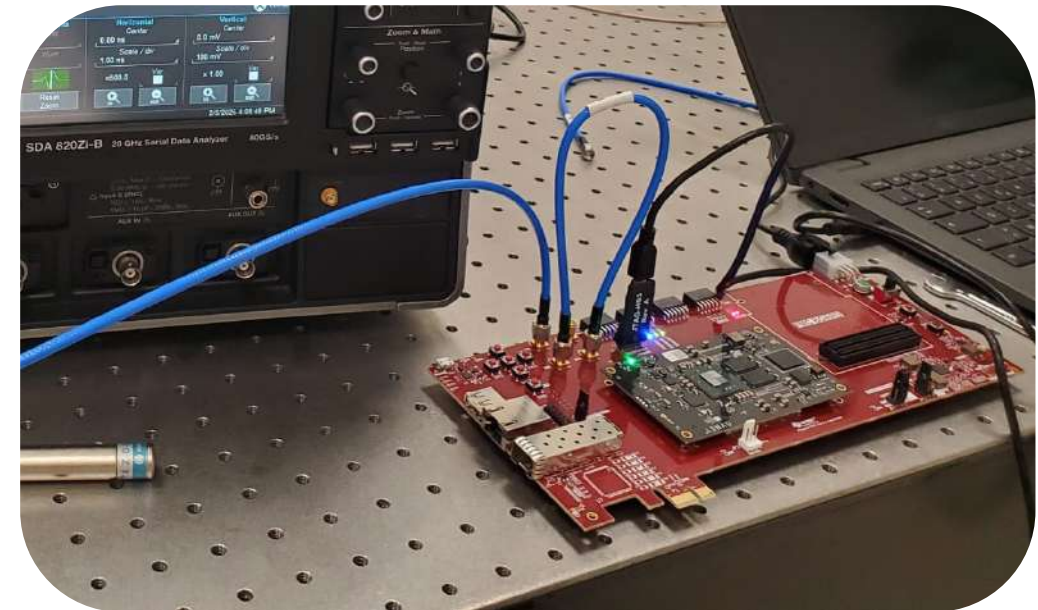
Supported by



# An ambitious and exciting roadmap



- **Advanced demo** under development
- **Pre-industrialization** ongoing
- **Collaboration** with big scaler under definition
- **Seed round** under preparation



elaia > EARLYBIRD

OVNI

VERVE  
VENTURES



The revolution has started: be part of it

72 Blackwell GPUs  
1.4 ExaFLOPS TE FP4

576 Memory Chips  
14 TB  
1.2 PB/s

18 NVLink Switches  
130 TB/s All-to-All

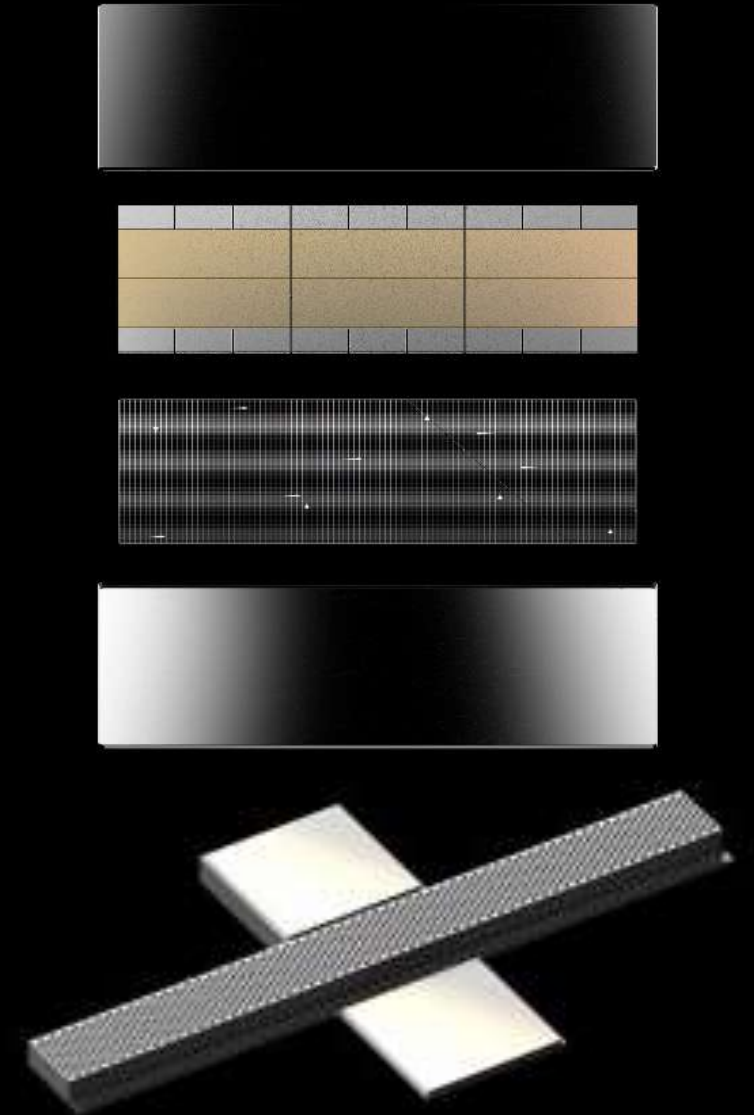
Grace Blackwell NVLink72

130 Trillion Transistors

2,592 Grace CPU Cores

72 ConnectX-8 NICs

18 BlueField DPUs





Illuminating the future of computing

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[www.ncodin.com](http://www.ncodin.com)